gate terminal of said thyristor device by a first terminal of said second semiconductor switch; second terminals of said first and second semiconductor switches being connected together,

wherein said first and second semiconductor switches are arranged such that [a signal of a first type applied to control electrodes of said first and second electronic switches turn said emitter turn-off thyristor to an on-state] and [a signal of a second type applied to control electrodes of said first and second electronic switches turn said emitter turn-off thyristor to an off-state].

34. An emitter turn-off thyristor as recited in claim 33, wherein said thyristor device and at [leasat] least one of said first and second semiconductor switches are formed monolithically.

35. [An emitter turn-off thyristor] as recited in claim 33 wherein [said thyristor device] and said first and second semiconductor switches are formed as discrete devices.

36. [An emitter turn-off thyristor] as recited in claim 35, wherein [said thyristor device] and said first and second semiconductor switches are commonly packaged.

37. An emitter turn-off thyristor as recited in claim 33, wherein at least one of said first and second semiconductor [devices] switches is an MOS device.

38. [An emitter turn-off thyristor] as recited in claim 33, wherein at least one of said first and second semiconductor switches is constituted by a plurality of semiconductor devices.